Flip-Flops and Sequential Circuit Design

ECE 152A – Summer 2009

Reading Assignment

- Brown and Vranesic
  - 7 Flip-Flops, Registers, Counters and a Simple Processor
    - 7.5 T Flip-Flop
      - 7.5.1 Configurable Flip-Flops
    - 7.6 JK Flip-Flop
    - 7.7 Summary of Terminology
    - 7.8 Registers
      - 7.8.1 Shift Register
      - 7.8.2 Parallel-Access Shift Register

Reading Assignment

- Brown and Vranesic (cont)
  - 7 Flip-Flops, Registers, Counters and a Simple Processor (cont)
    - 7.9 Counters
      - 7.9.1 Asynchronous Counters
      - 7.9.2 Synchronous Counters
      - 7.9.3 Counters with Parallel Load
    - 7.10 Reset Synchronization

Reading Assignment

- Brown and Vranesic (cont)
  - 7 Flip-Flops, Registers, Counters and a Simple Processor (cont)
    - 7.11 Other Types of Counters
      - 7.11.1 BCD Counter
      - 7.11.2 Ring Counter
      - 7.11.3 Johnson Counter
      - 7.11.4 Remarks on Counter Design

Reading Assignment

- Brown and Vranesic (cont)
  - 8 Synchronous Sequential Circuits
    - 8.1 Basic Design Steps
      - 8.1.1 State Diagram
      - 8.1.2 State Table
      - 8.1.3 State Assignment
      - 8.1.4 Choice of Flip-Flops and Derivation of Next-State and Output Expressions
      - 8.1.5 Timing Diagram
      - 8.1.6 Summary of Design Steps

Reading Assignment

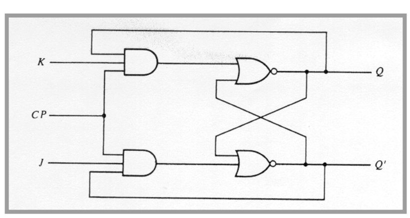
- Brown and Vranesic (cont)
  - 8 Synchronous Sequential Circuits (cont)
    - 8.2 State-Assignment Problem
      - One-Hot Encoding
    - 8.7 Design of a Counter Using the Sequential Circuit Approach
      - 8.7.1 State Diagram and State Table for Modulo-8 Counter
      - 8.7.2 State Assignment
      - 8.7.3 Implementation Using D-Type Flip-Flops
      - 8.7.4 Implementation Using JK-Type Flip-Flops
      - 8.7.5 Example – A Different Counter

Reading Assignment

- <u>Roth</u>
  - 11 Latches and Flip-Flops
    - 11.5 S-R Flip-Flop
    - 11.6 J-K Flip-Flop
    - 11.7 T Flip-Flop
    - 11.8 Flip-Flops with Additional Inputs
    - 11.9 Summary
  - 12 Registers and Counters
    - 12.5 Counter Design Using S-R and J-K Flip-Flops
    - 12.6 Derivation of Flip-Flop Input Equations – Summary

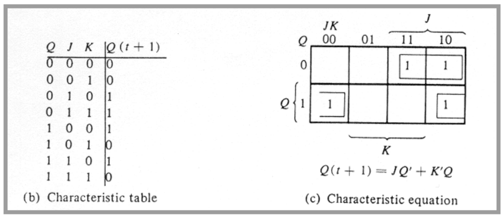
The JK Flip-Flop

- Allows J = K = 1 condition
  - Implemented with a gated SR latch and feedback of Q and Q*
    - Q toggles ($Q^+ = Q'$) on J = K = 1



The JK Flip-Flop (cont)

- Characteristic table and equation
  - Karnaugh map of characteristic table
  - Characteristic equation
    - $Q^+ = JQ' + K'Q$



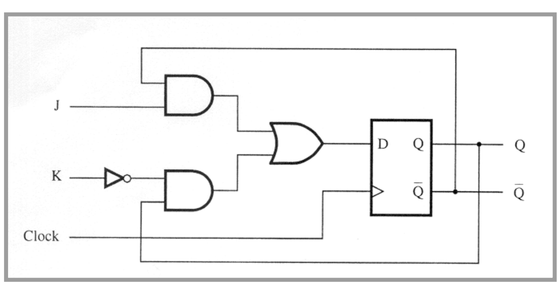
Q	J	K	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(b) Characteristic table

(c) Characteristic equation

The JK Flip-Flop (cont)

- Implementation using a D flip-flop
  - Characteristic Function at D input



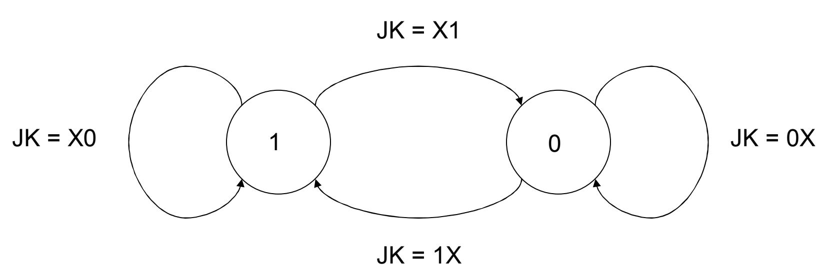
The JK Flip-Flop

- State table

	NS (Q^+)			
PS (Q)	JK = 00	01	10	11
0	0	0	1	1
1	1	0	1	0

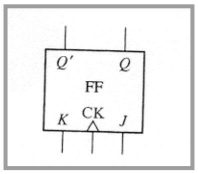
The JK Flip-Flop

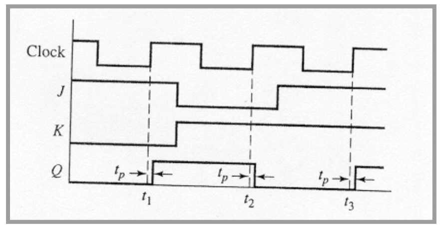
- State diagram



The JK Flip-Flop

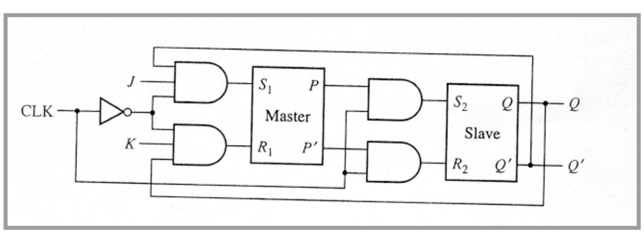
- With clock circuitry and timing
  - Positive edge triggered JK flip-flop





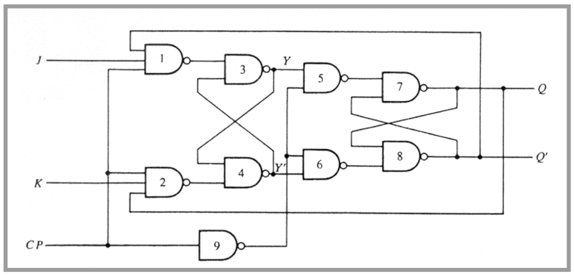
The Master Slave JK Flip-Flop

- Master Slave JK Flip-Flop
  - Rising edge triggered
    - note CLK inverted to master



The Master Slave JK Flip-Flop

- Master Slave JK Flip-Flop
  - Falling edge triggered
    - note CLK (CP) inverted to slave

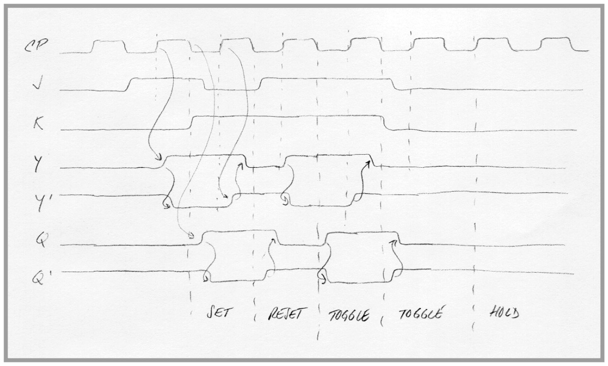


The Master Slave JK Flip-Flop

- Master active on CLK = 1
- Slave active on CLK = 0
  - Latch data in master on CLK = 1
  - Transfer data to slave (output) on CLK = 0
- Timing Diagram Initial Conditions
  - CLK = 0, J = 1, K = 0, Y = 0, Q = 0

The Master Slave JK Flip-Flop

- Timing Diagram



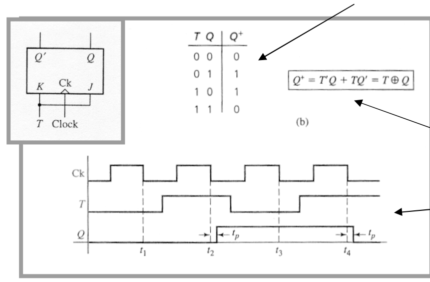
The JK Flip-Flop (cont)

- What happens if J = K = 1 for an indefinite period of time (i.e., much greater than clock period)?
  - Output oscillates at ½ the frequency of the clock
  - Divide by two counter

The T (Toggle or Trigger) Flip-Flop

- Connect J and K inputs together
  - Combined input "T"

Characteristic Table



Characteristic Equation

Timing Diagram

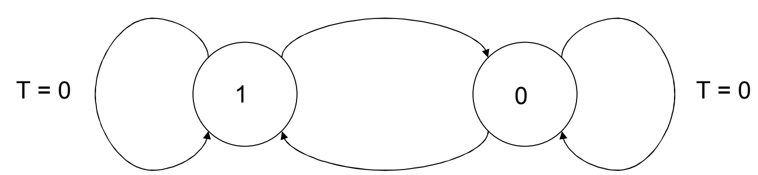
The T Flip-Flop

- State Table

	NS (Q^+)	
PS (Q)	T = 0	T=1
0	0	1
1	1	0

The T Flip-Flop

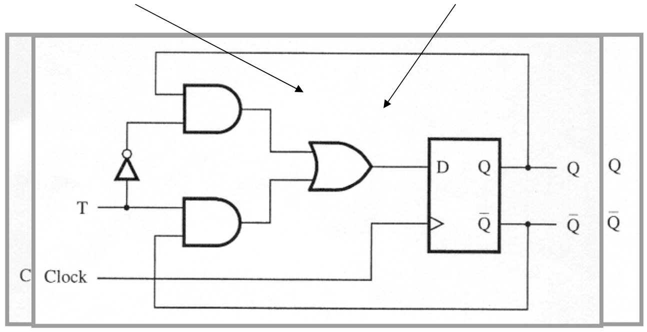
- State Diagram



The T Flip-Flop (from JK/D)

$Q^+ = JQ' + K'Q$

$Q^+ = T'Q + TQ' = T \text{ XOR } Q$

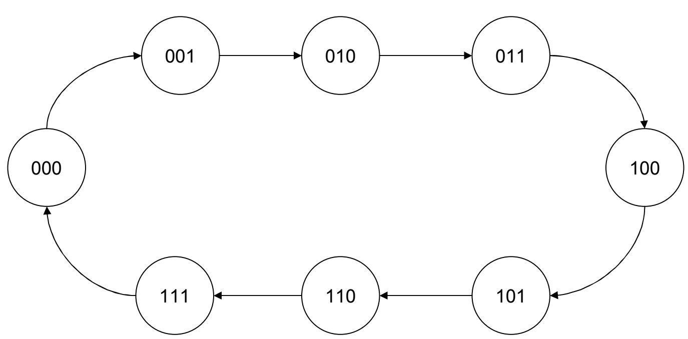


Counter Design with T Flip-Flops

- 3 bit binary counter design example
  - "State" refers to Q's of flip-flops
  - 3 bits, 8 states
    - Decimal 0 through 7
- No inputs
  - Transition on every clock edge
    - i.e., state changes on every clock edge
    - Assume clocked, synchronous flip-flops

Counter Design with T Flip-Flops

- State Diagram



Counter Design with T Flip-Flops

- State table

PS			NS		
A	B	C	A^+	B^+	C^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Counter Design with T Flip-Flops

- Next State Maps

A \ BC	00	01	11	10
0			1	
1	1	1		1

$A^+ = AB' + AC' + A'BC = D_A$

$B^+ = B'C + BC' = D_B$

$C^+ = C' = D_C$

A \ BC	00	01	11	10
0		1		1
1		1		1

A \ BC	00	01	11	10
0	1			1
1	1			1

Counter Design with T Flip-Flops

- Using D flip-flops, inputs are derived directly from next state maps
  - $D = Q^+$
- Using T flip flops
  - Excitation table (used for design)
    - $T = Q \text{ XOR } Q^+$
  - Need to find inputs to T flip-flops
    - Mapping state changes
      - $Q \rightarrow Q+$ requires T = ?

Counter Design with T Flip-Flops

- T Flip-Flop Excitation Table
  - $T = Q \text{ XOR } Q^+$

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

Counter Design with T Flip-Flops

- State Variable A
  - $T_A = A^+$ (XOR) A

A \ BC	00	01	11	10
A=0			$A^+ = 1$	
A=1	$A^+ = 1$	$A^+ = 1$		$A^+ = 1$

$A^+ = AB' + AC' + A'BC = D_A$

A \ BC	00	01	11	10
0			T=1	
1			T=1	

$T_A = BC$

Counter Design with T Flip-Flops

- State Variable B
  - $T_B = B^+$ (XOR) B

A \ BC	00 (B=0)	01 (B=0)	11 (B=1)	10 (B=1)
0		$B^+ = 1$		$B^+ = 1$
1		$B^+ = 1$		$B^+ = 1$

$B^+ = B'C + BC' = D_B$

A \ BC	00	01	11	10
0		T=1	T=1	
1		T=1	T=1	

$T_B = C$

Counter Design with T Flip-Flops

- State Variable C
  - $T_C = C^+$ (XOR) C

A \ BC	00 (C=0)	01 (C=1)	11 (C=1)	10 (C=0)
0	$C^+ = 1$			$C^+ = 1$
1	$C^+ = 1$			$C^+ = 1$

$C^+ = C' = D_C$

A \ BC	00	01	11	10
0	T=1	T=1	T=1	T=1
1	T=1	T=1	T=1	T=1

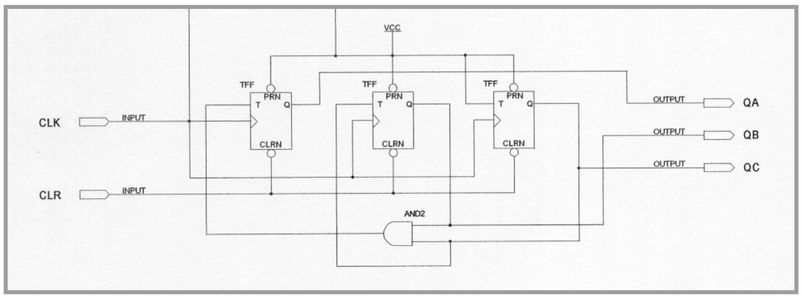
$T_C = 1$

Counter Design with T Flip-Flops

- Implement design using T Flip-Flops with asynchronous preset and clear
  - Asynchronous preset (PRN) and clear (CLRN) override clock and other inputs
    - Preset : Q → 1, Clear : Q → 0
    - Used to initialize system (all flip-flops) to known state
      - Bubbles indicate “low true” or “active low”
  - TA = BC, TB = C, TC = 1

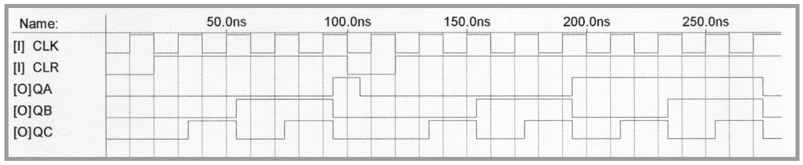
Counter Design with T Flip-Flops

- Schematic



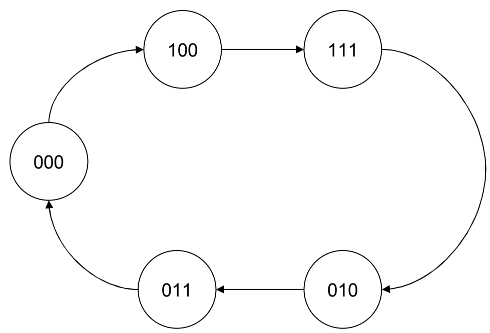
Counter Design with T Flip-Flops

- Timing Diagram
  - QA toggles when B = C = 1
  - QB toggles when C = 1
  - QC toggles on every clock edge



Counter Design with JK Flip-Flops

- State Diagram



Counter Design with JK Flip-Flops

- State Table

PS			NS		
A	B	C	A^+	B^+	C^+
0	0	0	1	0	0
0	0	1	X	X	X
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	X	X	X
1	1	0	X	X	X
1	1	1	0	1	0

Counter Design with JK Flip-Flops

- Next State Maps

A \ BC	00	01	11	10
0	1	X		
1	1	X		X

A \ BC	00	01	11	10
0		X		1
1	1	X	1	X

A \ BC	00	01	11	10
0		X		1
1	1	X		X

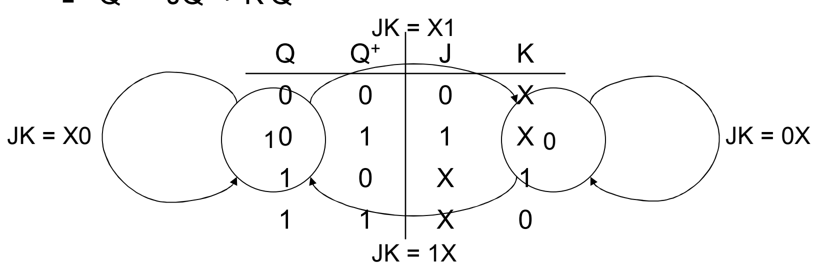
$A^+ = B' = D_A$

$B^+ = A + BC' = D_B$

$C^+ = AB' + BC' = D_C$

Counter Design with JK Flip-Flops

- JK Flip-Flop Excitation Table
  - Recall JK state diagram
  - Create excitation table from state diagram
    - $Q^+ = JQ' + K'Q$



Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Counter Design with JK Flip-Flops

- State Variable A
  - $A^+ = B'$

A \ BC	00	01	11	10
A=0	$A^+=1$	$A^+=X$		
A=1	$A^+=1$	$A^+=X$		$A^+=X$

A \ BC	00	01	11	10
0	1	X	0	0
1	X	X	X	X

$J_A = B'$

A \ BC	00	01	11	10
0	X	X	X	X
1	0	X	1	X

$K_A = B$

Counter Design with JK Flip-Flops

- State Variable B
  - $B^+ = A + BC'$

A \ BC	00	01	11	10
0	0	X	X	X
1	1	X	X	X

$J_B = A$

A \ BC	B=0: 00	B=0: 01	B=1: 11	B=1: 10
0		$B^+=X$		$B^+=1$
1	$B^+=1$	$B^+=X$	$B^+=1$	$B^+=X$

A \ BC	00	01	11	10
0	X	X	1	0
1	X	X	0	X

$K_B = A'C$

Counter Design with JK Flip-Flops

- State Variable C
  - $C^+ = AB' + BC'$

A \ BC	00 ($C=0$)	01 ($C=1$)	11 ($C=1$)	10 ($C=0$)
0		$C^+=X$		$C^+=1$
1	$C^+=1$	$C^+=X$		$C^+=X$

A \ BC	00	01	11	10
0	0	X	X	1
1	1	X	X	X

$J_C = A + B$

A \ BC	00	01	11	10
0	X	X	1	X
1	X	X	1	X

$K_C = 1$